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JC835 U.S. PTO 05/26/00

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PTO/SB/05 (4/98)
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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))

Attorney Docket No.	PD-99W166
First Inventor or Application Identifier	Linder
Title	"Low Noise, Low Distortion, Muxable*
Express Mail Label No.	EK444529150US

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

ADDRESS TO: **Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231**

1. [X] * Fee Transmittal Form *(e.g., PTO/SB/17)* *(Submit an original and a duplicate for fee processing)*
2. [X] Specification [*Total Pages* 13]
   (preferred arrangement set forth below)
   - Descriptive title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings *(if filed)*
   - Detailed Description
   - Claim(s)
   - Abstract of the Disclosure
3. [X] Drawing(s) *(35 U.S.C. 113)* [*Total Sheets* 6]
4. Oath or Declaration [*Total Pages* 3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 C.F.R. § 1.63(d)) *(for continuation/divisional with Box 16 completed)*
      i. [ ] DELETION OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).

** NOTE FOR ITEMS 1 & 13: IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C.F.R. § 1.27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C.F.R. § 1.28).*

5. [ ] Microfiche Computer Program *(Appendix)*
6. Nucleotide and/or Amino Acid Sequence Submission *(if applicable, all necessary)*
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

7. [X] Assignment Papers (cover sheet & document(s))
8. [X] 37 C.F.R.§3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
9. [ ] English Translation Document *(if applicable)*
10. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
11. [ ] Preliminary Amendment
12. [X] Return Receipt Postcard (MPEP 503) *(Should be specifically itemized)*
13. [ ] * Small Entity Statement(s) *(PTO/SB/09-12)* [ ] Statement filed in prior application, Status still proper and desired
14. [ ] Certified Copy of Priority Document(s) *(if foreign priority is claimed)*
15. [ ] Other: *Gilbert Mixer Signal Processing System and Method with AGC Functionality"

16. **If a CONTINUING APPLICATION,** *check appropriate box, and supply the requisite information below and in a preliminary amendment:*

[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: _____/_____

Prior application information: *Examiner* _____ *Group / Art Unit:* _____

For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.

17. CORRESPONDENCE ADDRESS

[ ] *Customer Number or Bar Code Label* *(Insert Customer No. or Attach bar code label here)* *or* [X] *Correspondence address below*

Name	Leonard A. Alkov, Esq. Raytheon Company				
Address	P.O. Box 902 (E1/E150)				
City	El Segundo	*State*	CA	*Zip Code*	90245-0902
Country	U.S.A.	*Telephone*	310.647.2577	*Fax*	310.647.2616

Name (Print/Type)	Leonard A. Alkov	*Registration No. (Attorney/Agent)*	30,021
Signature	Leonard A Alkov	*Date*	05/26/00

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Attorney Docket No. PD-99W166 *PATENT*

LOW NOISE, LOW DISTORTION, MUXABLE GILBERT MIXER SIGNAL PROCESSING SYSTEM AND METHOD WITH AGC FUNCTIONALITY

Lloyd F. Linder
Clifford N. Duong
Don C. Devendorf

LOW NOISE, LOW DISTORTION, MUXABLE GILBERT MIXER SIGNAL PROCESSING SYSTEM AND METHOD WITH AGC FUNCTIONALITY

This invention was made with Government support under Contract No. F30602-97-C-0223 awarded by the Air Force. The Government has certain rights in this invention.

BACKGROUND OF THE INVENTION

Field of the Invention:

The present invention relates to electronic circuits and systems. More specifically, the present invention relates to radio frequency receivers and transceivers used in communication applications.

Description of the Related Art:

For future military and commercial applications there may be a need for a radio capable of operating over a wide band of frequencies. This would ordinarily involve switching or multiplexing the received signal to one of N channels for subsequent gain control and mixing operations. However, it would be difficult for a single radio frequency (RF) switch to cover either the RF of IF frequency range.

Accordingly, a more promising approach would be to use a number of RF switches to selectively direct a received RF signal to an appropriate intermediate frequency processing stage. These switches would typically be single pole, multi-throw solid state switches implemented in silicon or Gallium Arsenide (GaAs). The switches would typically be disposed on a separate chip relative to the RF receiver in a 50-ohm environment.

Unfortunately, in addition to requiring complicated circuitry, this approach would present difficult power, third order intercept (intermodulation product distortion), noise figure, insertion loss and interchannel isolation issues. In addition, the switches would have to operate over a wide RF band or a wide IF band, both of which are difficult to achieve.

Hence, there is a developing need in the art for a system or method for providing a radio capable of operating over a wide band with minimal power consumption and circuit complexity. More specifically, there is a growing need in the art for a system or method for switching or multiplexing a received signal to one of N channels for subsequent gain control and mixing operations for individual and simultaneous output via a single stage at low power.

SUMMARY OF THE INVENTION

The need in the art is addressed by the signal processing system and method of the present invention. The inventive system includes a first circuit for distributing an input signal between two or more channels in a current mode of operation. A second circuit is disposed in each of the channels for processing the input signal and providing an output signal in response thereto. A third circuit is provided to combine the signals output by the processing circuit. A fourth circuit is included for controlling the first and the third circuits.

In a specific illustrative embodiment, the system further includes a radio frequency stage for downconverting a received signal and providing the input signal in response thereto. In the specific embodiment, the first circuit includes a mixing circuit. The mixing circuit includes Gilbert cells and circuitry for providing automatic gain control for each of the channels individually. The Gilbert cells and the automatic gain control circuitry are driven by a transconductance amplifier and therefore operate in a current mode. Differential digital automatic gain control signals are provided in response to a channel select signal from a digital control circuit. The inventive circuit

provides multiple IF channels which may be filtered individually. The invention thereby provides wide band operation in a simple low power single stage while the current mode thereof is effective in the reduction of insertion loss.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram of an illustrative implementation of a receiver incorporating the signal processing system of the present invention.

Fig. 2 is a block diagram showing an illustrative implementation of the mixing circuit of Fig. 1 in accordance with the present teachings.

Fig. 3 is a diagram showing an illustrative implementation of the digital automatic gain control circuit in more detail.

Fig. 4 is a diagram showing an illustrative implementation of the channel select multiplexer.

Fig. 5 is a diagram showing automatic gain control circuits, Gilbert cells, transconductance amplifier and load resistors of the mixer of Fig. 1 in more detail.

Fig. 6 is a schematic diagram of an illustrative implementation of an automatic gain control circuit of Fig. 5.

Fig. 7 is a schematic diagram of an illustrative implementation of a Gilbert cell of Fig. 5.

Fig. 8 is a block diagram of an illustrative implementation of the local oscillator multiplexer.

DESCRIPTION OF THE INVENTION

Illustrative embodiments and exemplary applications will now be described with reference to the accompanying drawings to disclose the advantageous teachings of the present invention.

While the present invention is described herein with reference to illustrative embodiments for particular applications, it should be understood that the invention is not limited thereto. Those having ordinary skill in the art and access to the teachings provided herein will recognize additional modifications, applications, and embodiments within the scope thereof and additional fields in which the present invention would be of significant utility.

Fig. 1 is a block diagram of an illustrative implementation of a receiver incorporating the signal processing system of the present invention. The system 10 includes an RF front end comprising an antenna 12, a conventional preselect filter 14, a low noise amplifier (LNA) 16 and an image rejection filter 18. The preselect filter 14 narrows the receive band down to the band of interest. Signals in the band of interest are amplified by the LNA 16 and images therein are rejected by the image rejection 0filter 18.

In accordance with the present teachings, the output of the image rejection filter 18 is applied to a mixing circuit 20 designed in accordance with the present teachings. The mixer 20 is controlled by a digital controller 30. The digital controller 30 may be implemented with software in a microprocessor, a serial controller, a field programmable gate array, application specific integrated circuit or suitable discrete logic. Those skilled in the art will appreciate that the present teachings are not limited to the use of a digital AGC circuit nor are the present teachings limited to a digital controller. Other suitable analog equivalents may be used for this purpose depending on the requirements of a given application.

The controller 30 provides mixer, RF automatic gain control (AGC), and RF channel select signals to the mixer 20.

Fig. 2 is a block diagram showing an illustrative implementation of the mixing circuit of Fig. 1 in accordance with the present teachings. As shown in Fig. 2, the mixing circuit 20 includes a digital automatic gain control circuit (DAGC) 70, which provides global gain control of the signal output by the filter 18.

Fig. 3 is a diagram showing an illustrative implementation of the digital automatic gain control circuit in more detail. The DAGC 70 may be implemented with a digital-to-analog converter (DAC) 72 and a transconductance (voltage to current) amplifier 74. The DAGC 70 outputs a gain controlled current control signal to a channel select multiplexer 80.

Fig. 4 is a diagram showing an illustrative implementation of the channel select multiplexer. The channel select multiplexer 80 may be implemented with a plurality of switches 82, 84, 86, 88 and 89 each of which receive the output of the DAGC 80 and output a differential automatic gain control current control signal in response to an associated channel select signal supplied by the controller 30 of Fig. 1.

Returning to Fig. 2, the differential outputs of the channel select multiplexer 80 are applied to a respective automatic gain control (AGC) circuit in a bank of AGCs 90 in the mixing circuit 20. The AGCs 90 control the current therethrough in response to the control signal received thereby from the DAGC 70 via the channel select multiplexer 80. All but one of the AGCs in the bank of AGCs 90 are connected to an associated Gilbert cell in a bank of Gilbert cells 100. The cells 100 receive a local oscillator signal from a local oscillator source 40 (Fig. 1) via a local oscillator multiplexer 110. Current for the Gilbert cells 100 is supplied by a second transconductance amplifier 120 and adjusted by the AGCs 90 in proportion to the signal supplied by the DAGC 70.

Fig. 5 is a diagram showing automatic gain control circuits, Gilbert cells, transconductance amplifier and load resistors of the mixer of Fig. 1 in more detail. The system 10 is implemented with five channels. Those skilled in the art will appreciate that the present teachings are not limited to the number of channels employed. In theory, the number of IF sections that can be added will depend on the effects of the parasitic capacitance at the MUX/AGC stage at the RF stage output, and the effect on the bandwidth of the local oscillator driver. A long as adding more stages does not band limit the local oscillator severely or band limit the RF signal path (or degrade the intercept performance there), then more stages can be added until such events occur.

Each channel pushes differential current through the second transconductance amplifier 120 and includes an AGC 92, 94, 96, 98 or 99.

In the illustrative embodiment, the transconductance amplifier 120 is implemented with first and second bipolar (NPN) transistors 121 and 122 connected in an emitter degenerated differential pair configuration. The collector of each transistor 121 and122 provides one of the two differential inputs to each of the AGCs 90. The base terminals of the first transistor 121 and the second transistor 122 in the amplifier 120 are supplied by a bias supply via first and second resistors 123 and 124, respectively. The emitter terminals of the first transistor 121 and the second transistor 122 in the amplifier 120 are connected to ground via first and second current sources 125 and 126, respectively. In addition, the emitter terminals of the first transistor 121 and the second transistor 122 are connected via a resistor 127. In addition, the base terminal of the second transistor 122 is filtered by a capacitor 128 connected to ground.

As mentioned above, the gain of the current through each of the AGCs 90 is set by the gain control signal supplied by the controller 30 via the DAGC 70. Each AGC is selected via the multiplexer 80 by a channel select signal supplied by the controller 30 as described above.

Fig. 6 is a schematic diagram of an illustrative implementation of an automatic gain control circuit of Fig. 5. The gain control circuits may be implemented in accordance with the teachings of U.S. Patent No. 6,040,731 issued March 21, 2000, to Chen *et al.* and entitled **Differential Pair Gain Control Stage**, the teachings of which are incorporated herein by reference. In the illustrative implementation, each AGC (e.g. 99) includes, for each input, a first bipolar (NPN) transistor 152 and a second transistor 153 (or 154 and 155) connected in a differential pair configuration to receive an AGC control signal (e.g., AGC5) from the DAGC 70 as mentioned above. The emitter terminals of each transistor pair are connected to one of the differential inputs from the transconductance amplifier 120. One transistor in each pair 153 and 154 is connected to a source of supply voltage (V_{cc}) via a bias resistor 156 or 157, respectively. The collector terminals of the second transistor in each pair 152 and 155 provide the differential outputs of the AGC.

Channels 1, 2, 4 and 5 include a Gilbert cell 102, 104, 108 and 109 respectively. Gilbert cells are well known in the art. See for example U. S. Patent No. 3,689,752 issued 09/05/72 to Barrie Gilbert and entitled **Four Quadrant Multiplier Circuit**, the teachings of which are incorporated herein by reference.

Fig. 7 is a schematic diagram of an illustrative implementation of a Gilbert cell of Fig. 5. Each cell (e.g., 109) includes a pair of transistors 162/164 and 166/168 for each differential input connected in a Differential pair configuration. Each base terminal of each transistor in each pair is connected to and LO in Figure 5, which is generated in the LO MUX 110 in Figure 2, which creates the multiple LO signals in Figure 8.

The emitter terminals of the two transistors in each pair are connected to one of the differential inputs from an associated AGC. The collector terminal of each transistor in each pair is tied to a collector terminal of the other pair and provides one of the differential outputs of the cell.

As mentioned above, the cells 100 receive a local oscillator signal from a local oscillator source 40 (Fig. 1) via a local oscillator multiplexer 110.

Fig. 8 is a block diagram of an illustrative implementation of the local oscillator multiplexer. The local oscillator multiplexer 110 includes a 2:1 multiplexer 170 which receives internal local oscillator (LO) and external LO inputs from the local oscillator source 40 of Fig. 1 and a 1 bit select input from the digital controller 30. The LO source 40 can be either generated internally on the chip in a phase lock loop (PLL) (defined as INTERNAL LO), or externally off the chip (EXTERNAL LO). The output of the multiplexer 170 is provided to a 1:4 demultiplexer 174 via an isolation and squaring circuit 172. A digital circuit 176 provides two bit LO select control for the 1:4 demultiplexer 174. Digital circuit 176 is a two-bit decode, and can be part of the control circuit 30. I did not receive Figure 9 in the packet. The DMUX 174 is in Figure 8, and it is a conventional design. Two digital bits select one of the four paths (the fifth path is a by-pass mode).

The demultiplexer 174 provides input to each of four local oscillator drivers 178, 180, 182 and 184. Each driver may be of conventional design and includes squaring circuitry as is common in the art. The four drivers 178, 180, 182 and 184 output LO1, LO2, LO4 and LO5 which are used to drive the Gilbert cells 102, 104, 108 and 109 of Fig. 5 respectively.

The AGC 96 in the third channel draws differential gain controlled current from an RF amplifier 106 consisting in the illustrative embodiment of two DC biased transistors 105 and 107 arranged in a cascode configuration.

The differential outputs of the Gilbert cells 102, 104, 108 and 109 and the RF amplifier 106 draw current from the source V_{cc} via an associated load resistor R_L for the transconductance amplifier 120. Differential outputs for each channel are provided at the connection with the associated load resistor R_L. The Gilbert cells mix the local oscillator signal and the RF signal from the AGC circuits to provide differential outputs

for each channel at the local oscillator frequency plus or minus the radio frequency: LO + RF and LO - RF.

Returning to Fig. 1, as discussed above, the mixing circuit 20 provides a 1:N multiplexing of the output of the filter 18 to one of several channels in response to a local oscillator 40 and signals from the controller 30. That is, the output of the mixer 20 is distributed to one of N channels (where N = 5 in the illustrative embodiment of Fig. 1). In each channel, a filter 45, 46, 47, 48 or 49 is disposed. The filters 45, 46, 47, 48 and 49 are intermediate frequency (IF) filters which pass signals over various bandwidths at various frequencies as required for a given multi-band application.

The outputs of the filters are combined by an N:1 demultiplexer 50 and input to an intermediate frequency (IF) amplifier 52. The output of the IF amplifier 52 is processed by an anti-aliasing filter 54 and digitized by an analog-to-digital converter (ADC) 56. The output of the ADC is input to a signal processor 58 which outputs to a personal computer (PC) 60 or other output device as may be appropriate for a given application. The signal processor 58 provides control signals for the system 10 via the digital controller 30. That is, in accordance with the present teachings, the signal processor 58 provides channel select, AGC select and local oscillator select control signals for the system 10 via the digital controller 30. The signal processor can do fast Fourier transforms on the received signal, correlate a spread spectrum PN-code, demodulate the received signal, determine chirp rates of received signals, etc. The signal processor is application specific, to perform the necessary processing for a given application. The PC 60 allows for selective display of the information output by the signal processor 58 and/or additional data processing.

The system 10 may be implemented on a single application specific integrated circuit (ASIC). Those skilled in the art will appreciate that flexibility is built into the ASIC, through the multiplexing function, providing the ability to use off-chip inductive-capacitive (LC) or surface acoustic wave (SAW) filters, or on-chip active filters.

In addition, the system may be implemented with a by-pass mode, by which the received signal is not mixed to an IF frequency, but passes instead directly through on-chip (to IF circuitry prior) to an external ADC. The added multiplexing capability of the AGC/low voltage Gilbert mixer allows this flexibility without compromising performance. A key to this performance feature is due to the fact that multiplexing is accomplished in current mode in the RF signal path on-chip.

Since the MUX is integrated in current mode in the RF path, additional measures can be taken to help the isolation. In the case of this architecture, the local oscillator, for the unused channels is blanked so that RF leakage will not mix into the IF bandwidth of interest.

Thus, the present invention has been described herein with reference to a particular embodiment for a particular application. Those having ordinary skill in the art and access to the present teachings will recognize additional modifications, applications and embodiments within the scope thereof.

It is therefore intended by the appended claims to cover any and all such applications, modifications and embodiments within the scope of the present invention.

Accordingly,

WHAT IS CLAIMED IS:

CLAIMS

1. A signal processing system comprising:

first means for distributing an input signal between two or more channels in a current mode of operation;

second means disposed in each of said channels for processing said input signal and providing an output signal in response thereto;

third means for combining the signals output by said processing means; and

fourth means for controlling said first and said third means.

2. The invention of Claim 1 further including a radio frequency stage for downconverting a received signal and providing said input signal in response thereto.

3. The invention of Claim 1 wherein said first means includes a mixing circuit.

4. The invention of Claim 3 wherein said mixing circuit further includes means for providing automatic gain control for each of said channels individually.

5. The invention of Claim 4 wherein said means for providing automatic gain control operates in a current mode.

6. The invention of Claim 5 wherein said means for providing automatic gain control includes a digital automatic gain control circuit.

7. The invention of Claim 6 further including means for selectively providing differential digital automatic gain control signals in response to a channel select signal.

8. The invention of Claim 3 wherein said mixing circuit further includes means for mixing said input signal with a mixing signal.

9. The invention of Claim 8 wherein said mixing circuit operates in a current mode.

10. The invention of Claim 9 wherein said mixing circuit further includes means for mixing said input signal with plural mixing signals.

11. The invention of Claim 10 wherein said mixing circuit includes at least one Gilbert cell.

12. The invention of Claim 11 wherein said mixing circuit includes a transconductance amplifier.

13. The invention of Claim 12 wherein said mixing circuit includes an automatic gain control circuit.

14. The invention of Claim 1 wherein said second means includes first and second filters disposed in a first and a second of said channels respectively.

15. A receiver comprising:

a radio frequency stage for downconverting a received signal and providing said input signal in response thereto;

first means for distributing said input signal between two or more channels in a current mode of operation, said first means including a mixing circuit having

a Gilbert cell for each channel,

an automatic gain control circuit for each channel in communication with a respective one of said Gilbert cells, and

a transconductance amplifier in communication with said automatic gain control circuits;

second means disposed in each of said channels for processing said input signal and providing an output signal in response thereto, second means including first and second filters disposed in a first and a second of said channels respectively;

third means for combining the signals output by said processing means; and

fourth means for controlling said first and said third means.

16. A signal processing method comprising the steps of:

distributing an input signal between two or more channels in a current mode of operation;

processing said input signal and providing an output signal in response thereto;

combining the signals output by said processing means; and

controlling said first and said third means.

ABSTRACT OF THE DISCLOSURE

A signal processing system and method. The inventive system includes a first circuit for distributing an input signal between two or more channels in a current mode of operation. A second circuit is disposed in each of the channels for processing the input signal and providing an output signal in response thereto. A third circuit is provided to combine the signals output by the processing circuit. A fourth circuit is included for controlling the first and the third circuits. In a specific illustrative embodiment, the system further includes a radio frequency stage for downconverting a received signal and providing the input signal in response thereto. In the specific embodiment, the first circuit includes a mixing circuit. The mixing circuit includes Gilbert cells and circuitry for providing automatic gain control for each of the channels individually. The Gilbert cells and the automatic gain control circuitry are driven by a transconductance amplifier and therefore operate in a current mode. Differential digital automatic gain control signals are provided in response to a channel select signal from a digital control circuit. The inventive circuit provides multiple IF channels which may be filtered individually. The invention thereby provides wide band operation in a simple, single stage implementation that consumes little power. Further, the current mode thereof is effective in the reduction of insertion loss.

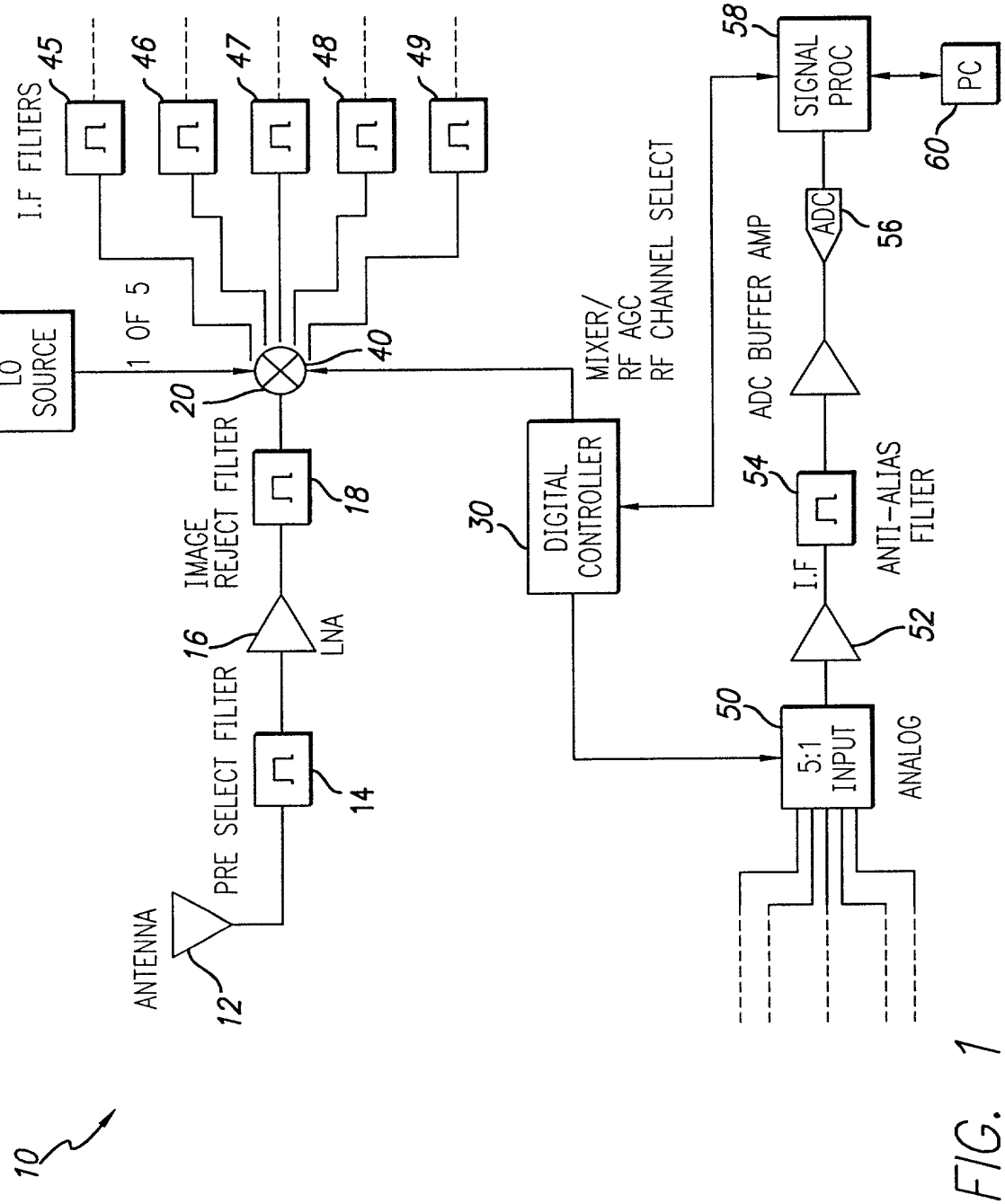
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FIG. 1

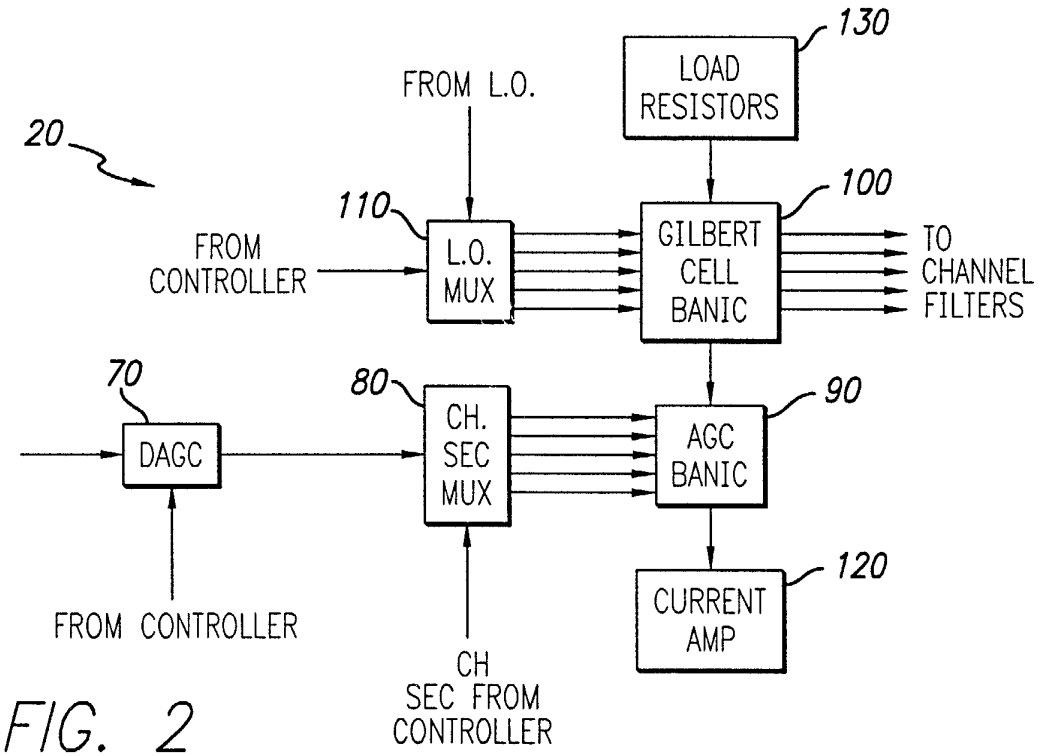
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FIG. 2

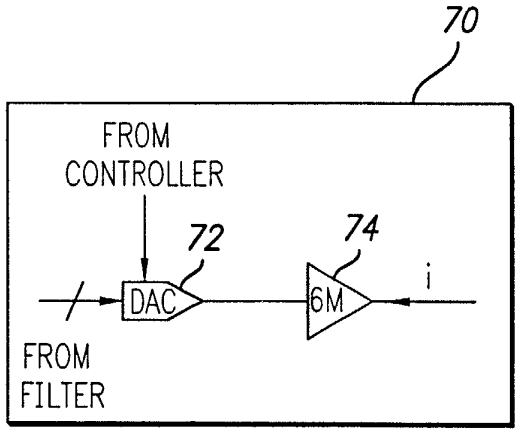
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FIG. 3

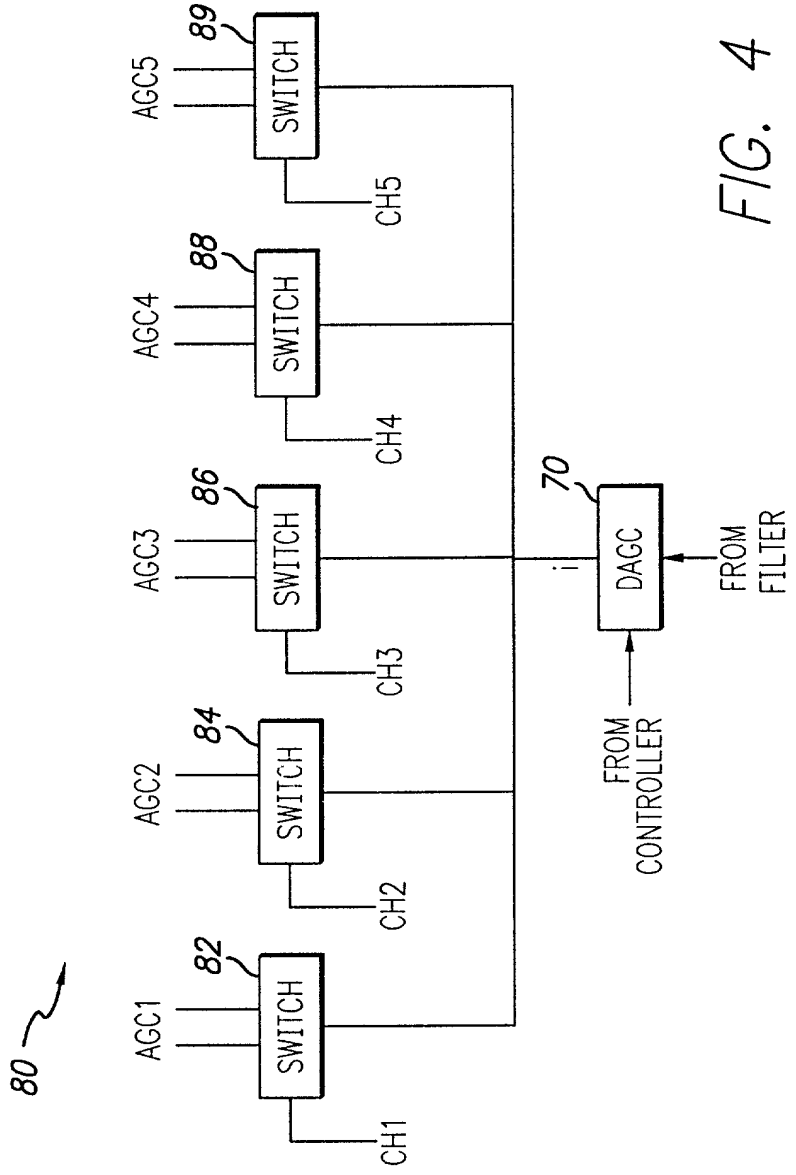
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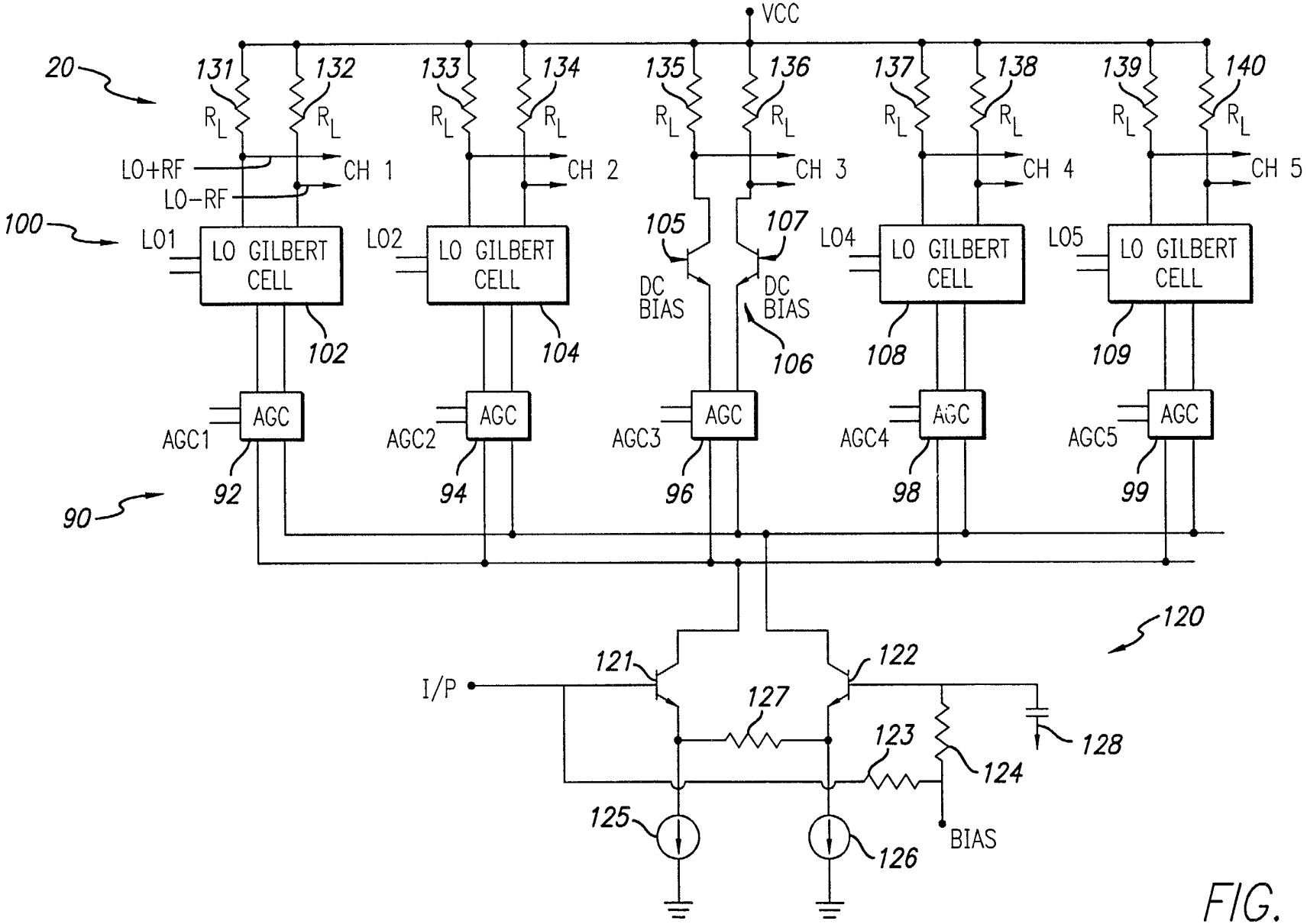
FIG. 4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LO1
LO2
LO4
LO5
LO GILBERT CELL
105
107
DC BIAS
102
104
106
108
109
AGC
AGC1
AGC2
AGC3
AGC4
AGC5
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124
128
125
126
BIAS

FIG. 5

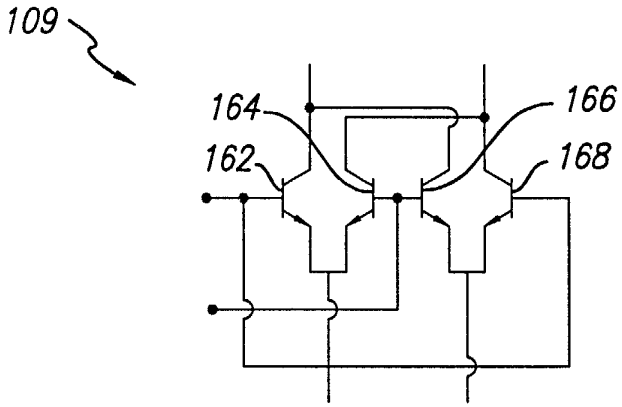


FIG. 7

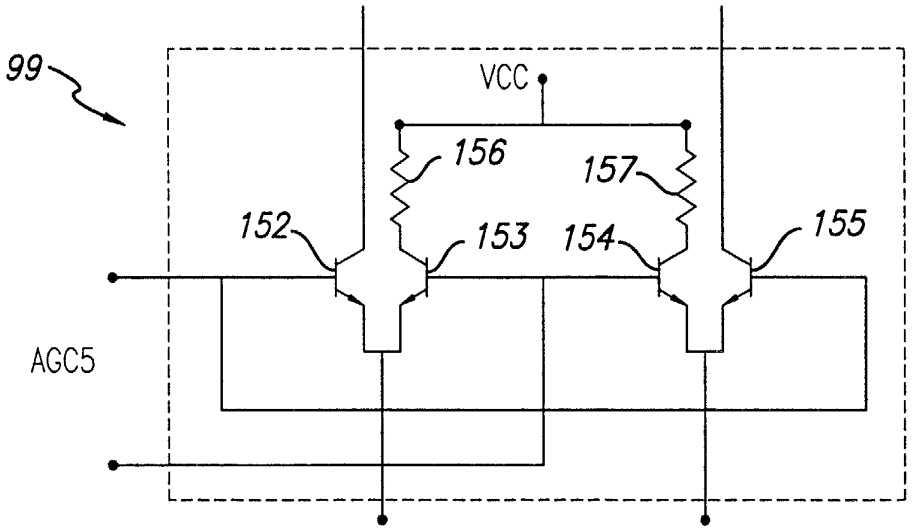
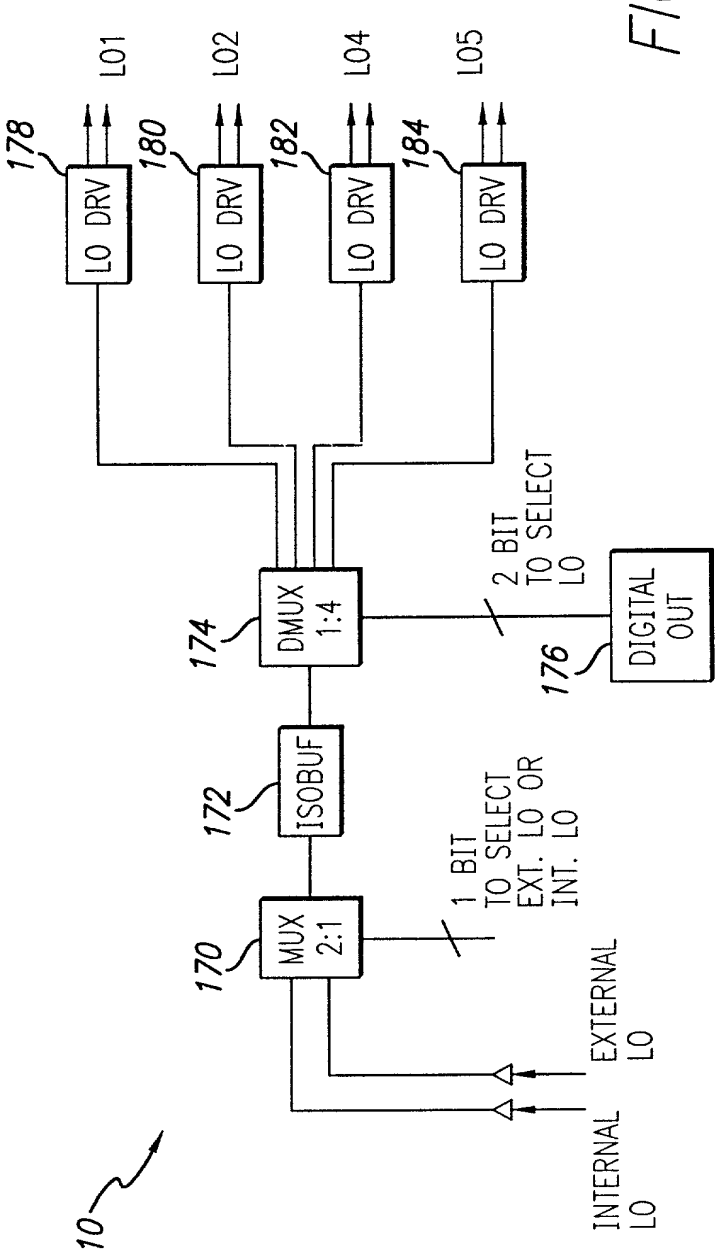


FIG. 6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DMUX 1:4
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LO DRV
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FIG. 8

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DECLARATION FOR UTILITY OR DESIGN PATENT APPLICATION (37 CFR 1.63)

[X] Declaration Submitted with Initial Filing OR [ ] Declaration Submitted after Initial Filing (surcharge (37 CFR 1.16 (e)) required)

Attorney Docket Number	PD-99W166
First Named Inventor	Linder
COMPLETE IF KNOWN	
Application Number	/
Filing Date	
Group Art Unit	
Examiner Name	

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

"Low Noise, Low Distortion, Muxable Gilbert Mixer Signal Processing System and Method with AGC Functionality"

(Title of the Invention)

the specification of which
[X] is attached hereto
OR
[ ] was filed on (MM/DD/YYYY) [ ] as United States Application Number or PCT International Application Number [ ] and was amended on (MM/DD/YYYY) [ ] (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment specifically referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT international application which designated at least one country other than the United States of America, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or of any PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application Number(s)	Country	Foreign Filing Date (MM/DD/YYYY)	Priority Not Claimed	Certified Copy Attached? YES	NO
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]
			[ ]	[ ]	[ ]

[ ] Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto:

I hereby claim the benefit under 35 U.S.C. 119(e) of any United States provisional application(s) listed below.

Application Number(s)	Filing Date (MM/DD/YYYY)

[ ] Additional provisional application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

Burden Hour Statement: This form is estimated to take 0.4 hours to complete. Time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.

Please type a plus sign (+) inside this box → [+]

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DECLARATION — Utility or Design Patent Application

I hereby claim the benefit under 35 U.S.C. 120 of any United States application(s), or 365(c) of any PCT international application designating the United States of America, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application.

U.S. Parent Application or PCT Parent Number	Parent Filing Date (MM/DD/YYYY)	Parent Patent Number *(if applicable)*

☐ Additional U.S. or PCT international application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached hereto.

As a named inventor, I hereby appoint the following registered practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☐ Customer Number [ ] → *Place Customer Number Bar Code Label here*
OR
☐ Registered practitioner(s) name/registration number listed below

Name	Registration Number	Name	Registration Number
Leonard A. Alkov	30,021		
Glenn H. Lenzen, Jr.	29,320		
Colin M. Raufer	40,781		
William C. Schubert	30,102		

☐ Additional registered practitioner(s) named on supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: ☐ Customer Number or Bar Code Label [ ] *OR* ☒ Correspondence address below

Name	Leonard A. Alkov, Esq.				
Address	Raytheon Company				
Address	P.O. Box 902 (E1/E150)				
City	El Segundo	**State**	CA	**ZIP**	90245-0902
Country	USA	**Telephone**	310.647.2577	**Fax**	310.647.2616

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor: ☐ A petition has been filed for this unsigned inventor

Given Name (first and middle [if any])	Family Name or Surname
Lloyd F.	Linder

Inventor's Signature	Lloyd F. Linder					**Date**	05/18/00
Residence: City	Agoura Hills	**State**	CA	**Country**	USA	**Citizenship**	USA
Post Office Address	3730 Patrick Henry						
Post Office Address							
City	Agoura Hills	**State**	CA	**ZIP**	91301	**Country**	USA

☒ Additional inventors are being named on the 1 supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto

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DECLARATION

ADDITIONAL INVENTOR(S)
Supplemental Sheet
Page 3 of 3

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor
Given Name (first and middle [if any])	Family Name or Surname
Clifford N.	Duong

Inventor's Signature	Cliff Duong					Date	05/23/02
Residence: City	Fountain Valley	State	CA	Country	USA	Citizenship	USA
Post Office Address	9119 La Estrella Avenue						
Post Office Address							
City	Fountain Valley	State	CA	ZIP	92708	Country	USA

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor
Given Name (first and middle [if any])	Family Name or Surname
Don C.	Devendorf

Inventor's Signature	Don C Devendorf					Date	5/10/02 5/13/02
Residence: City	Carlsbad	State	CA	Country	USA	Citizenship	USA
Post Office Address	2016 Caracol Court						
Post Office Address							
City	Carlsbad	State	CA	ZIP	92009	Country	USA

Name of Additional Joint Inventor, if any:	☐ A petition has been filed for this unsigned inventor
Given Name (first and middle [if any])	Family Name or Surname

Inventor's Signature						Date	
Residence: City		State		Country		Citizenship	
Post Office Address							
Post Office Address							
City		State		ZIP		Country	

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